

**WHAT IS CLAIMED IS:**

- 1     1. An apparatus, comprising:  
2         a semiconductor substrate;  
3         a first conducting layer in contact with the semiconductor substrate, the first conducting  
4     layer comprising a base layer metal, the base layer metal comprising Cu;  
5         a diffusion barrier in contact with the first conducting layer;  
6         a wetting layer on top of the diffusion barrier; and  
7         a bump layer on top of the wetting layer, the bump layer comprising Sn, the Sn bump  
8     layer being electroplated, the diffusion barrier being adapted to prevent Cu and Sn from  
9     diffusing through the diffusion barrier.  
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11    2.     The apparatus of Claim 1, wherein the diffusion barrier is an electroless diffusion  
12    barrier.  
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14    3.     The apparatus of Claim 1, further comprising a solder layer positioned between the  
15    bump layer and a die package, wherein the solder layer comprises Sn.  
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17    4.     The apparatus of Claim 1, wherein the base layer metal comprises an adhesion layer  
18    and a seed layer, wherein the adhesion layer comprises one of Ti, TiN, and TiSiN, and the  
19    seed layer comprises one of Ni, NiV, and Co.  
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21    5.     The apparatus of Claim 4, wherein the base layer metal further comprises a metal  
22    layer positioned between the adhesion layer and the seed layer, wherein the metal layer  
23    comprises Al.  
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25    6.     The apparatus of Claim 1, wherein the diffusion barrier comprises one of CoBP,  
26    CoWP, CoWB, CoWBP, NiBP, NiWP, NiWB, and NiWBP, wherein the bump layer further  
27    comprises a Sn alloy, the Sn alloy comprising one of 0.7Cu, Bi, Sb, and 3.5Ag, wherein the  
28    Sn bump layer being electroplated is further adapted to prevent low temperature phase  
29    transition of Sn from alpha Sn into beta Sn.  
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31 7. The apparatus of Claim 1, wherein the wetting layer comprises one of CoB, NiB, and  
32 NiP, wherein the diffusion barrier is further adapted to reduce bump layer delamination.

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34 8. The apparatus of Claim 1, wherein the apparatus further comprises a sputtered base  
35 layer metal, wherein the diffusion barrier is further adapted to reduce electromigration related  
36 to CuSn intermetallic formation.

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38 9. An apparatus comprising:  
39 a base layer metal on a semiconductor substrate, the base layer metal comprising Cu;  
40 a bump layer on top of the base layer metal, the bump layer comprising an  
41 electroplated Cu layer;  
42 a diffusion barrier in contact with the bump layer;  
43 a wetting layer on top of the diffusion barrier; and  
44 a solder layer contacting the bump layer, the solder layer comprising Sn, the diffusion  
45 barrier being further adapted to prevent the diffusion of Cu and Sn through the diffusion  
46 barrier.

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48 10. The apparatus of Claim 9, wherein the diffusion barrier comprises an electroless  
49 diffusion layer.

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51 11. The apparatus of Claim 9, wherein the base layer metal comprises an adhesion layer  
52 and a seed layer, wherein the adhesion layer comprises one of Ti, TiN, and TiSiN, and the  
53 seed layer comprises one of Ni, NiV, and Co.

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55 12. The apparatus of Claim 10, wherein the base layer metal further comprises a metal  
56 layer positioned between the adhesion layer and the seed layer, wherein the metal layer  
57 comprises Al, wherein the diffusion barrier is adapted to suppress a whisker-type formation  
58 in the bump layer.

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60 13. The apparatus of claim 12, wherein the base layer metal further contacts the diffusion  
61 barrier to physically isolate all surfaces of the bump layer from the solder layer.

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63 14. The apparatus of claim 9, wherein the diffusion barrier comprises one of CoBP,  
64 CoWP, CoWB, CoWBP, NiBP, NiWP, NiWB, and NiWBP, wherein the wetting layer  
65 comprises one of CoB, NiB, and NiP.  
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67 15. A method comprising:  
68 performing passivation with SiN and polyimide;  
69 depositing a base layer metal;  
70 depositing a photoresist layer;  
71 forming a diffusion barrier, the diffusion barrier being adapted to prevent intermixing of  
72 Cu and Sn between different layers;  
73 forming a wetting layer on top of the diffusion barrier;  
74 forming a bump layer;  
75 removing the photoresist layer; and  
76 etching the base layer metal.  
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78 16. The method of Claim 15, wherein the depositing the base layer metal comprises one  
79 of a plasma vapor deposition (PVD), a chemical vapor deposition (CVD), and an atomic  
80 layer deposition (ALD), wherein the diffusion barrier comprises an electroless diffusion  
81 barrier.  
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83 17. The method of Claim 16, wherein the base layer metal comprises an adhesion layer  
84 and a seed layer, wherein the adhesion layer comprises one of Ti, TiN, and TiSiN, and the  
85 seed layer comprises one of Ni, NiV, and Co, wherein the electroless diffusion barrier is  
86 further adapted to reduce bump layer delamination.  
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88 18. The method of Claim 17, wherein depositing the base layer metal comprises  
89 depositing a metal layer positioned between the adhesion layer and the seed layer, wherein  
90 the base layer metal further comprises one or more electrical interconnects..  
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19. The method of Claim 18, wherein the metal layer comprises Al, wherein the photoresist layer is adapted for patterning, wherein the electroless diffusion barrier is further adapted to reduce electromigration related to CuSn intermetallic formation.

20. The method of Claim 16, wherein the electroless diffusion barrier comprises one of CoBP, CoWP, CoWB, CoWBP, NiBP, NiWP, NiWB, and NiWBP.

21. The method of Claim 16, wherein the bump layer comprises Sn, the Sn being electroplated to prevent low temperature phase transition of Sn from alpha Sn into beta Sn, wherein the Sn being electroplated is further adapted to suppress whisker formation.

22. The method of Claim 16, wherein the bump layer comprises a Sn alloy, the Sn alloy comprising one of 0.7Cu, Bi, Sb, and 3.5Ag, wherein the Sn alloy is electroplated to prevent low temperature phase transition of Sn from alpha Sn into beta Sn.

23. The method of Claim 16, further comprising:  
forming a solder layer to the bump layer, the solder layer comprising Sn; and  
connecting a die package to the solder layer.

24. A method comprising:  
performing passivation with SiN and polyimide;  
depositing a base layer metal;  
depositing a photoresist layer;  
forming a Cu layer, the Cu layer being electroplated;  
forming an electroless diffusion barrier, the electroless diffusion barrier being positioned between the Cu layer and a Sn layer, the electroless diffusion barrier being adapted to prevent Cu and Sn from diffusing through the electroless diffusion barrier;  
forming a wetting layer on top of the electroless diffusion barrier;  
removing the photoresist layer; and  
etching the base layer metal.

123 25. The method of Claim 24, further comprising forming a solder region on top of the  
124 wetting layer and the electroless diffusion barrier, wherein the solder region is in contact with  
125 a die package, wherein the solder region comprises Sn.

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127 26. The method of Claim 24, wherein the Sn layer comprises a solder region on top of the  
128 electroless diffusion barrier, wherein the solder region is in contact with a die package.

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130 27. The method of Claim 24, wherein the electroless diffusion barrier comprises one of  
131 CoBP, CoWP, CoWB, CoWBP, NiBP, NiWP, NiWB, and NiWBP.

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133 28. A method comprising:  
134 performing passivation with SiN and polyimide;  
135 depositing a base layer metal;  
136 depositing a photoresist layer;  
137 forming a bump layer, the bump layer comprising Cu, the Cu bump layer being  
138 electroplated;  
139 removing the photoresist layer;  
140 etching the base layer metal;  
141 forming an electroless diffusion barrier layer, the electroless diffusion barrier layer being  
142 positioned between the Cu bump layer and a Sn layer, the electroless diffusion barrier layer  
143 being adapted to prevent intermixing of Cu and Sn between different layers; and  
144 forming a wetting layer on top of the electroless diffusion barrier layer.

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146 29. The method of Claim 28, wherein the electroless diffusion barrier layer comprises one  
147 of CoBP, CoWP, CoWB, CoWBP, NiBP, NiWP, NiWB, and NiWBP, wherein the base layer  
148 metal comprises an adhesion layer and a seed layer, wherein the adhesion layer comprises  
149 one of Ti, TiN, and TiSiN, and the seed layer comprises one of Ni, NiV, and Co.

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151 30. The method of Claim 28, wherein the base layer metal further physically contacts the  
152 electroless diffusion barrier layer, wherein the bump layer comprises an outer surface,

153 wherein the outer surface of the bump layer is physically isolated from contacting a layer  
154 comprising Sn.

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156 31. The method of Claim 28, wherein the Cu bump layer is further adapted to prevent  
157 formation of whisker formation, wherein the electroless diffusion barrier layer is further  
158 adapted to reduce electromigration related to CuSn intermetallic formation.

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160 32. A system having a circuit board comprising:  
161 one or more components comprising circuitry; and  
162 one or more layers on the circuit board to route at least one signal between components  
163 on the circuit board, wherein at least one of the components on the circuit board comprises a  
164 die packing interconnect comprising:  
165 a semiconductor substrate;  
166 a first conducting layer in contact with the semiconductor substrate, the first  
167 conducting layer comprising a base layer metal, the base layer metal comprising Cu;  
168 a diffusion barrier in contact with the first conducting layer;  
169 a wetting layer on top of the diffusion barrier; and  
170 a bump layer on top of the wetting layer, the bump layer comprising Sn, the Sn bump  
171 layer being electroplated, the diffusion barrier being adapted to prevent Cu and Sn from  
172 diffusing through the diffusion barrier.

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174 33. The system of Claim 32, wherein the one or more components comprise any one of a  
175 central processing unit, a memory, and a logic unit.